From Automated Verification
to Automated Design
(Invited Talk Abstract)

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One of the most significant developments in the area of design verification over the last decade is the development of of algorithmic methods for verifying temporal specification of finite-state designs (Clarke, Grumberg, and Peled 1999). A frequent criticism against this approach, however, is that verification is done after significant resources have already been invested in the development of the design. Since designs invariably contains errors, verification simply becomes part of the debugging process. The critics argue that the desired goal ought to be the use of the specification in the design development process in order to guarantee the development of correct designs. This is called design synthesis (Church 1957; Pnueli and Rosner 1989). In this talk I will review 50 years of research on the design-synthesis problem and show how the automata-theoretic approach can be used to solve it (Kupferman and Vardi 2005; Pnueli and Rosner 1989; Rabin 1972).

References

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