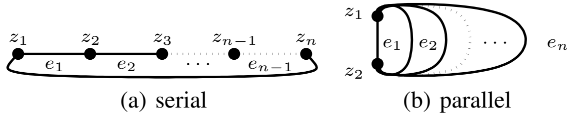

(a) serial (b) parallel

Figure 4: Serial and parallel graph topologies

Predicted Topological Reduction

This section examines the type of topological reduction that is possible for a typical model. We focus on two key topologies, serial and parallel sub-graphs, as shown in figure 4(a).[2] We assume we have a topology graph in which parallel edges are allowed, e.g., for system redundancy. The size of a graph $G(V, E)$ is denoted in terms of the number of edges, i.e., $|G| = |E|$. The size of $G(V, E)$ is essential to the algorithmic performance of algorithm 3 as it is equal to the size of the nodal matrix.

Definition 6 (Contraction Operators). Given a graph $G(V, E)$ and an edge $e = \{v, w\}$, the graph $G'(V', E') = G(V, E) \searrow e$ is such that $E' = E \backslash \{e \cup F\}$, $V' = V \backslash v$, F is the set of all edges that are parallel to $\{v, w\}$, and each edge $\{x, v\} \in E$ such that $x \neq w$ is replaced with an edge $\{x, w\} \in E'$.

Given a graph $G(V, E)$ and an edge e, the graph $G'(V', E') = G(V, E) \nwarrow e$ is such that $E' = E \backslash e$, $V' = V \backslash \{W \cup v\}$ where v is incident to e and W is the set of singly connected vertices in $E \backslash v$.

We have chosen the symbols $\searrow$ and $\nwarrow$ to visually resemble the set exclusion operator \ as the two contraction operators decrease the size of G. The graph contraction ratio, for graphs with at least on edge, is:

$$\rho = \frac{\sum_{e \in E} \left[|G \searrow e| + |G \nwarrow e| \right]}{2\,|G|^2} \tag{2}$$

The variable ρ in eq. 2 adds-up the effect of applying $\searrow$ and $\nwarrow$ to each edge in E. Note that $\rho \in [0; 1]$. The denominator in eq. 2 is simply $|G(V, E)|$-times the number of edges in $G(V, E)$. The coefficient is 2 in the denominator because we have two contraction operators: $\searrow$ and $\nwarrow$. In graphs with a single loop, $\rho = 0$, i.e., the sum of the sizes of all contracted graphs is zero.

Lemma 1. *The following two statements are true:*

1. *The total graph contraction for a serial graph $G(V, E)$ with edges $E = \{\{z_1, z_2\}, \{z_2, z_3\}, \ldots, \{z_{n-1}, z_n\}\}$ is $\rho = \frac{1}{2}$.*
2. *The total graph contraction for a parallel graph $G(V, E)$ with edges $E = \{\{z_1, z_2\}, \{z_1, z_2\}, \ldots, \{z_1, z_2\}\}$ is $\rho = \frac{1}{2}$.*

Proof (Sketch). In a graph $G(V, E)$ with serial topology, there are exactly $G(V, E) = |E| = n$ edges as illustrated in figure 4(a). Choose any edge e. Applying $\searrow$ to e removes only e from the original graph $G(V, E)$ and results in:

$$\sum_{e \in E} |G \searrow e| = n\,(n-1) \tag{3}$$

On the other hand, applying $\nwarrow$ to e, regardless of the choice of e results in a singly-connected graph:

$$\sum_{e \in E} |G \nwarrow e| = n \tag{4}$$

Substituting eq. 3 and eq. 4 into eq. 2 gives us $\rho = \frac{n + n(n-1)}{2n^2}$ which simplifies to $\rho = \frac{1}{2}$. The correctness of statement 2 can be proven in a similar manner. □

We now prove a theorem that predicts how algorithm 3 affects a class of random graphs; in the following section we empirically validate our theoretical predictions. Our random graphs depict serially connected circuits with random connections. We generate our random graphs by adding random edges to a serially connected graph such as the one shown in figure 4(a). This structure of augmenting regular graphs with random edges is the standard method for random-graph generators, and is known to closely match the structure of real-world systems (da F. Costa et al. 2007).

In the following, we denote the average graph degree of a graph $G(V, E)$ as $\bar{d} = 2|E|/|V|$.

Theorem 1. *The total graph contraction for a serially-connected generated graph $G(V, E)$ is $\rho = k\bar{d}$.*

Proof (Sketch). We decompose $G(V, E)$ into two graphs: $G(V, E')$ and $G(V, E'')$ where E' is the set of random edges and $G(V, E'')$ is a serially connected graph. This decomposition is possible due to the way $G(V, E)$ is constructed. Let $G(V, E'')$ consists of C components (the computation of C is shown in Erdős and Rényi (1960)). We can now show that the overall reduction $\rho = k_1 \rho' + k_2 \rho''$ will be the average of reducing $G(V, E')$ and $G(V, E'')$. From lemma 1, $\rho'' = \frac{1}{2}$. Finally, both k_1 and k_2 are proportional to $\bar{d}$, hence $\rho = k'_1 \bar{d} \rho' + k''_2 \bar{d} \rho''$. As there is no dependency between k'_1, k''_1, ρ', and ρ'' (ρ'' depends on C only), then we can conclude that ρ is proportional to the average graph degree. □

Although there is an analytical method to obtain ρ for generated graphs, we compute it experimentally which also shows the absolute improvement in computational complexity due to the symbolic preprocessing. We do this in the following section.

Experiments

Algorithms 1–3 are implemented as a part of the (deleted for anonymity) diagnostic framework.

Benchmark

No benchmark for analogue linear circuits exists, to the best of our knowledge, unlike digital circuit benchmarks, e.g., (Brglez and Fujiwara 1985). Consequently, we have generated the circuits that we need.

[2] We plan to address additional sub-graphs in future work.

Name	N	variables	|COMPS|
N-SERIAL	3–202	11–608	3–202
N-PARALLEL	3–202	9–407	3–202
N-MIXED	3–102	18–513	6–204
N-MESH	3–12	48–723	18–288
N-TREE	3–5	57–6253	27–3125

Table 1: Circuit benchmark

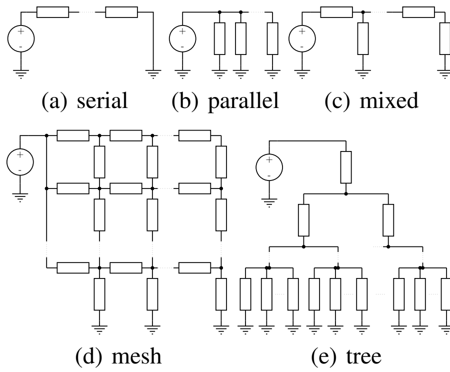

Figure 5: Scalable circuits with regular topology used for performance analysis

Table 1 shows a number of regular circuits. These topologies can be scaled by setting a variable N, producing a range of circuit sizes.

All benchmark circuits have a single voltage source that cannot fail. The N-SERIAL circuits, shown in figure 5(a), consist of N resistors connected in series. Similarly, the N-PARALLEL circuits in figure 5(b) consist of N resistors connected in parallel. The N-MIXED topology is a combination of N-SERIAL and N-PARALLEL as shown in figure 5(c). The N-MESH circuits consist of $2 \times N^2$ resistors arranged in a rectangular grid as shown in figure 5(d). Finally, the N-TREE circuits are complete N-ary trees of depth N. They are shown in figure 5(e).

For N-SERIAL, $\bar{d} = 2$. For N-PARALLEL, $\bar{d} = N + 1$. For N-MIXED, $\bar{d} = (4N + 2)/(N + 2)$ which approaches 4 for larger N. The N-MESH circuits have average graph degree $\bar{d} = (4N^2{+}2)/(N^2{+}2)$ which approaches 4 when increasing N even faster than N-MIXED.

In addition to the regular circuits from the preceding section we have created 6 370 "generated" circuits that have realistic topological properties. We generate these circuits by adapting the random graph algorithm proposed by Sedgewick (2002, p. 42). We modify the original algorithm to ensure multiple graph components for sparse graphs.

We generate graphs by specifying the vertex/edge ratio r. The relation between the graph generation parameter r and the average graph density $\bar{d}$ is given by $|E| = rN + C - 1$, where C is the number of connected components in G. From the fact that $|V| = N$ it follows that $\bar{d} = 2Nr + C - 1/N$. For our experiments we have chosen $0.1 \leq r \leq 0.4$ which translates to $2.06 \leq \bar{d} \leq 2.9$.

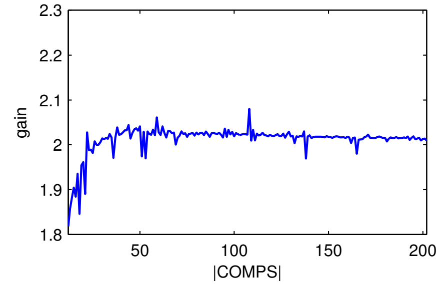

Figure 6: N-SERIAL performance gain

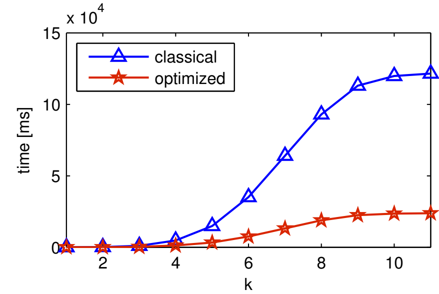

Figure 7: 11-SERIAL k-fault performance

Results

Figure 6 shows the ratio of the CPU time of the optimized versus the non-optimized algorithm. The performance gain due to the graph preprocessing is close to 2.02, does not depend on the circuit size, and is almost constant (there is some measurement noise).

The performance gain for N-PARALLEL is the same as for N-SERIAL. Not surprisingly, algorithm 3 helps only a little in the connected topologies of figure 5(c) and figure 5(d). For these two dense topologies, we have measured a performance gain of at most 9%. The reason for this is that a single faulty component decreases the size of the nodal matrix by one.

The most significant benchmark performance gain due to algorithm 3 is for k-fault simulations where $k > 1$. The performance of the diagnostic search decreases exponentially with k, except when k approaches N because then the nodal matrix is almost degenerate, hence easier to decompose. On the other hand, multiple faults increase the frequency with which significant parts of the nodal graphs are pruned. For example, when $k = 2$, an open-circuit close to the voltage source in N-SERIAL makes N simulations use a 2×2 matrix instead of the normal $N \times N$.

The performance gain due to k-fault simulations is shown in figure 7. In order to simulate k-fault combinations, we have chosen a small $N = 11$. The performance gain increases for larger k and reaches a factor of 5.12 for $k = 12$.

Figure 8 shows the average algorithm complexity with random circuits. On the x-axis we have the number of nodes in the topology graph. The y-axis is the number of edges coefficient r. The z-axis shows the ratio of the time of the diagnosis with and without algorithm 3.

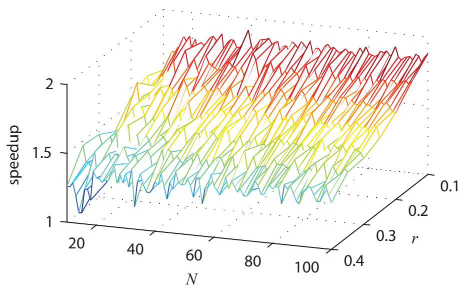

Figure 8: Performance gain for random circuits of various size and with varying density

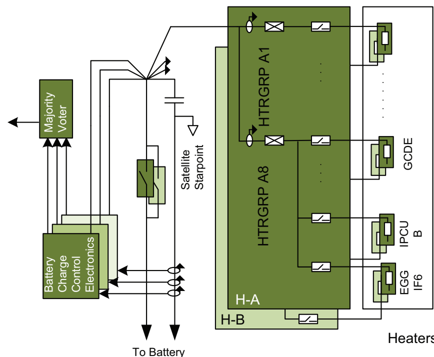

Figure 9: The design of the satellite EPS is highly redundant to increase reliability

Figure 8 shows that the performance gain due to algorithm 3 does not depend on the circuit size, i.e., it is almost constant. What determines the performance gain is the edge density. For $r = 0.1$ we have almost twice speed improvement and it decreases to ≈ 1.25 for $r = 0.4$. The performance gain is bounded from below by the performance gain of the N-SERIAL topology due to the nature of random graph generation algorithm.

The linear correlation coefficient of the speedup shown in figure 8 and the average graph degree is -0.89 which validates the analysis in section . The negative sign in the correlation is due to the fact that r defined as the number of graph vertices per edge while $\bar{d}$ is reciprocal to r, i.e., $\bar{d}$ is defined as the number of edges per graph vertex.

We have a modeled the Electrical Power System (EPS) of a real-world satellite (Feldman et al. 2013). It consists of, amongst others, 96 heating elements (modeled as resistors), 112 switches (modeled as resistors whose resistor changes as a result of a user-supplied command), and approx. 1000 equations. Most components have at least two fault modes, in addition to the nominal one. The many switching components and the designed cold-redundancy lead to a large number of normally open-circuit or short-circuit elements at any given time. As a result, algorithm 3 leads to a performance speedup factor of at-least 38.9, and that is for the single fault assumption. For the double-fault assumption we have a performance gain of 194 times.
The reason for the very good performance of the symbolic reduction is in the highly regular and redundant design of the satellite EPS as is illustrated in figure 9. Consider, for example, the topology of the power distribution and heater network. The electrical heaters provide double redundancy and are grouped in lines of six. A fault assumption eliminates a whole line of resistors which, given, the cubic complexity of the simulation algorithm translates to the substantial savings that we have measured in our experiments.

The performance gain of symbolically pruning faulty components is even more expressed when assuming double-fault hypotheses (the latter increases diagnostic accuracy which is outside the scope of this work) or when using diagnostic inference as a subroutine in a more complex algorithm such as active testing (Feldman, Provan, and van Gemund 2010a). The double-fault assumptions decrease the size of the nodal matrix with more than 20% and there are many cases in which the nodal matrix becomes of trivial size (e.g., two faulty main distribution switches).

Related Work

Analog systems diagnosis is a well-studied area, and a variety of approaches have been developed, based on methods such as off-line numerical test-generation (Duhamel and Rault 1979), bond graph approaches (Samantaray et al. 2006), machine learning (Aminian and Aminian 2000), "intelligent" methods (Dague et al. 1992; Fenton, McGinnity, and Maguire 2001), and MODELICA fault models (Minhas et al. 2014). The domain of analogue systems that has received the most attention is that of fault diagnosis of analog circuits, e.g., (Bandler and Salama 1985; Kabisatpathy, Barua, and Sinha 2005; Milor 1998). Although much progress has been made, most prior work addresses only single-fault cases. Achievements towards automatic multiple-fault diagnosis are documented in, i.a., (Korzybski 2008; Liu and Starzyk 2002); however, many aspects of the problem are still open, and no fully-automatic method exists for multiple-fault generic analog circuit diagnosis.

In general, parametric-fault simulation-after-test (SAT) methods must be used to address the non-linear diagnostic equations. When the parameters differ only slightly beyond their tolerance ranges, the equation can be linearized (Tadeusiewicz and Hałgas 2006). For more significant differences, more accurate results for this task are needed. These include methods for solving nonlinear equations, e.g., the Newton-Raphson method or its variants (Cherubal and Chatterjee 1999; Navid and Willson, Jr. 1979), modified nodal approaches (Ho, Ruehli, and Brennan 1975), evolutionary algorithms (Augusto and Almeida 2000), or least square methods (Hongkui and Pengnian 1988).

Researchers have studied dynamic discontinuities in bond graphs (Mosterman and Biswas 1996). This paper complements the approach of Mosterman and Biswas by providing an algorithmic framework for dealing with structural (or parametric) discontinuities. Our approach is fully applicable to bond graphs (Mosterman and Biswas 1999).

Conclusions

In this paper we study the advantages of dynamically modifying the simulation model for steady-state analysis

in diagnosis. We show that speedups due to pruning of parametrized components that cause discontinuity in the model depend on the topology of the model, and empirically justify this theoretical prediction through extensive experimentation on a benchmark of circuits. Further, our method does not decrease the diagnostic accuracy.

We observe most computational savings in real-world circuits where, due to standard redundancy for fault-tolerance, there are many unpowered and shorted sub-circuits that can be pruned. We also observe that the computational performance increases with the number k of k-fault combinations.

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