Implementation of Boolean AND and OR Logic Gates with Biologically Reasonable Time Constants in Spiking Neural Networks

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Abstract

Latest developments in the field of power-efficient neural interface circuits provide an excellent platform for applications where power consumption is the primary concern. Developing neural networks to achieve pattern recognition on such hardware remains a daunting task owing to substantial computational complexity. We propose and demonstrate a Spiking Neural Network (SNN) with biologically reasonable time constants to implement basic Boolean Logic Gates. The same network can be further applied to more complex problem statements. We employ a frequency spike encoding for data representation in the model, and a simplified and computationally efficient model of a neuron with exponential synapses and Spike Timing Dependent Plasticity (STDP).

Introduction

Spiking Neural Networks (SNNs) (also called third generation of Artificial Neural Networks (ANNs)) are highly inspired by the Natural Computing in the brain. In contrast to the standard ANNs which utilize integer or real-valued inputs, SNNs process data in the form of series of very short impulses or activation potentials, also known as spike trains. A spike train is a single bit line switching temporally between logical levels of '0' and '1'. SNNs are therefore known to incorporate spatial as well as temporal information (Petrović 2013).

Electrical models provide an estimated imitation of a neuron cell. The classic leaky integrate-and-fire (LIF) model (Stoliar et al. 2017) and its generalized form, spike response model (SRM) (Ourdighi and Benyettou 2016) are widely used to represent neuron cells computationally. These models can be analyzed as analog components of charging and discharging RC circuit which can be computationally complex when expressed in digital systems. The SNN model presented in this paper is a feed-forward network. Hence the output of a signal has a different weighted potential contribution as it reaches to the last neuron. The input signal is encoded as a spike train and supplied to the input neurons.

The main characteristic of a spiking neuron is the membrane potential (MP). The transmission of a single spike from one neuron to another is mediated by the point where neurons interact. In neurobiology, a transmitting neuron is defined as a pre-synaptic neuron and a receiving neuron as a post-synaptic neuron. With no activity, neurons have a small electrical charge, known as the resting potential. When a single spike arrives at a post-synaptic neuron, it generates an excitatory post-synaptic potential (EPSP). The MP at an instant is calculated as the sum of all present PSPs at the neuron inputs. When the MP reaches a critical threshold value, a post-synaptic spike is sent out. After a refractory period, the neuron potential returns to its resting value and is ready to fire a new spike if MP is above the threshold.

Spiking neurons do not fire at each propagation cycle but only fire based on their membrane potential. The sum of individual spike trains generated by the pre-synaptic neurons changes the membrane potential of post-synaptic neurons.

In this proposed model, we combine spike encoding, the neuron membrane model, and the STDP learning. Since energy consumption is a significant cost factor, we use biologically plausible time constants and mechanism such as exponential synapse with STDP which can be easily used on neural interface circuits (Benjamin et al. 2014). Researchers (Reljan-Delaney and Wall 2017) have tried to model AND gates with SNNs but the results were not good. However, SNN gave good results for XOR problem. We propose that using biologically plausible time constants, we can build an SNN model for logical AND and OR gates efficiently. It was seen that the proposed model can accurately represents both the AND and OR gates.

Approach and Model

In the proposed Spiking Neural Network model STDP learning is employed where, there is a weight change if there is a pre-synaptic spike in the temporal vicinity of a post-synaptic spike. If the pre-synaptic spike occurs immediately before the post-synaptic spike, then the change is positive. Otherwise, the change is negative, as illustrated with the biological data from (Bi and Poo 2001). Thus, our interest lies in this temporal range only which induces a change in the synaptic weights. In our network, each connection between the two neurons is associated with a delay of d time units, which is the time difference between the post-synaptic firing time and the time the pre-synaptic potential starts rising. Since the model is envisioned to be used in digital systems, time is counted in discrete units. The membrane potential $P(t)$ is described as a function of time and is increased by a synap-

tic weight value w_i for each incoming spike. A constant value D is subtracted from the membrane potential at every time instant to take into account the delay of d time units. When the membrane potential crosses the threshold potential (P_{th}), the neuron produces a spike and the membrane potential decreases to the resting potential P_{ref} , which is the minimum potential level of a neuron. The process is described by Equation 1. The resulting EPSP function can be easily implemented with a register and a counter.

$$P(t) = \begin{cases} P(t-1) + \\ \sum_{i=1}^{n} w_i S_{it} - D, & if P_{min} < P_{t-1} < P_{th}. \\ P_{ref}, & if P_{t-1} \geq P_{th} \\ R_p, & if P(t-1) \leq P_{min} \end{cases} \quad (1)$$

R_p is the resting potential, i.e, the minimum potential at which a neuron stays without any pre-synaptic spike input. $P_{refract}$ is numerically the same as R_p, but it signifies an overloaded condition. This state occurs after a post-synaptic spike has been fired. After firing the spike, the neuron again returns to the minimum potential state. P_{min} is the minimum limit of the membrane potential. It is used to avoid any negative polarization of the neuron. An exponential curve, which is biologically more plausible with the neuromorphic hardware systems, is used for STDP learning. Equation 2 describes the learning function, where the constants A^+ and A^- determine the maximum excitation and inhibition values; and constants τ_p and τ_m determine the steepness of the function. Equation 3 represents the weight change equations, where w_{max} and w_{min} bound the weights and α controls the rate of weight change.

$$\Delta w = \begin{cases} A^+ exp(\frac{-\Delta t}{\tau_p}), & if \Delta t \geq 0; \\ -A^- exp(\frac{-\Delta t}{\tau_m}), & if \Delta t < 0 \end{cases} \quad (2)$$

$$w_{new} = \begin{cases} w_{old} + \alpha \Delta w(w_{max} - w_{old}), & if \Delta w > 0. \\ w_{old} + \alpha \Delta w(w_{old} - w_{min}), & if \Delta w \leq 0 \end{cases} \quad (3)$$

Results and Discussion

A model of SNN is proposed to implement OR and AND Boolean logic gates. Inputs to the network are rate coded using Poisson process spike generator. Random noise is added to mimic natural biological scenarios and each synaptic terminal is treated as a distinct connection with independent weights. Biologically plausible parameters were used for training and simulation (Jug 2012). The truth tables for OR and AND gate obtained by the SNN model is given in Figure 1. A simulation for logical AND gate is shown in Figure 2 for different inputs. Other necessary figures and explanations are given as supplementary files. From both the figures, it can be seen that post-synaptic spikes are only fired when membrane potential crosses the threshold. The network learned appropriate weights in just 100 iterations. Algorithms were written from scratch in Python on a 64-bit OS with 8 GB of RAM and an Intel i5-5200U processor.

x_1	x_2	y
0	0	0
0	1	0
1	0	0
1	1	1

Logical AND.

x_1	x_2	y
0	0	0
0	1	1
1	0	1
1	1	1

Logical OR.

Figure 1: Truth Tables Obtained for Different Inputs in the Proposed SNN Model

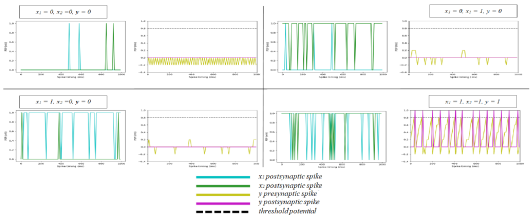

Figure 2: A Simulation of the SNN Model for Logical AND Gate

Conclusion

In this paper, we described a simple, biologically plausible and computationally efficient architecture of a spiking neuron network which is optimized for embedded system implementations. Learning is robust and stable. In future, we would like to implement the same biologically plausible and power efficient SNN architecture for more complex pattern recognition tasks and validate our results using them.

References

Benjamin, B. V.; Gao, P.; McQuinn, E.; Choudhary, S.; Chandrasekaran, A. R.; Bussat, J. M.; Alvarez-Icaza, R.; Arthur, J. V.; Merolla, P. A.; and Boahen, K. 2014. Neurogrid: A Mixed- Analog- Digital Multichip System for Large- Scale Neural Simulations. *Proceedings of the IEEE* 102(5):699–716.

Bi, G. Q., and Poo, M. M. 2001. Synaptic Modification by Correlated Activity: Hebb's Postulate Revisited. *Annual Review of Neuroscience* 24(1):139–166.

Jug, F. 2012. *On Competition and Learning in Cortical Structures*. Ph.D. Dissertation, ETH Zurich.

Ourdighi, A., and Benyettou, A. 2016. An Efficient Spiking Neural Network Approach based on Spike Response Model for Breast Cancer Diagnostic. *International Arab Journal of Information Technology* 13(3):1032–1038.

Petrović, C. 2013. *Spiking Neural Networks: Pattern Formation and Plasticity*. Verlag Nicht Ermittelbar.

Reljan-Delaney, M., and Wall, J. 2017. Solving the Linearly Inseparable XOR Problem with Spiking Neural Networks. In *Computing Conference*, 701–705. IEEE.

Stoliar, P.; Tranchant, J.; Corraze, B.; Janod, E.; Besland, M. P.; Tesler, F.; Rozenberg, M.; and Cario, L. 2017. A Leaky- Integrate- and- Fire Neuron Analog Realized with a Mott Insulator. *Advanced Functional Materials* 27(11):1604740.