

QiMeng-CRUX: Narrowing the Gap Between Natural Language and Verilog via Core Refined Understanding eXpression

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Abstract

Large language models (LLMs) have shown promising capabilities in hardware description language (HDL) generation. However, existing approaches often rely on free-form natural language descriptions that are often ambiguous, redundant, and unstructured, which poses significant challenges for downstream Verilog code generation. We treat hardware code generation as a complex transformation from an open-ended natural language space to a domain-specific, highly constrained target space. To bridge this gap, we introduce **Core Refined Understanding eXpression (CRUX)**, a structured intermediate space that captures the essential semantics of user intent while organizing the expression for precise Verilog code generation. We further design a two-stage training framework, comprising *Joint Expression Modeling* and *Dual-Space Optimization*, to enhance the quality of both CRUX and Verilog code. Experiments across multiple Verilog generation benchmarks demonstrate that our model, QiMeng-CRUX, achieves state-of-the-art performance among general models, particularly under challenging design tasks. Furthermore, the CRUX space proves transferable and beneficial when used as input prompts for other code models, highlighting its effectiveness in narrowing the gap between free-form natural language descriptions and precise Verilog generation.

Introduction

Large language models (LLMs) have shown remarkable progress in code generation for general-purpose programming languages, spurring increasing interest in automating hardware description language (HDL) code generation, such as Verilog (Chen et al. 2024). Recent efforts have substantially improved LLM performance on hardware design tasks through advancements in many aspects, such as data construction (Liu et al. 2024b; Zhao et al. 2025a; Zhang et al. 2024), feedback mechanisms (Wang et al. 2025a; Cui et al. 2024; Zhu et al. 2025), and training paradigms (Gao et al. 2024; Pei et al. 2024). However, most existing LLM-based methods for Verilog generation focus primarily on the code generation phase and rely solely on free-form natural language descriptions, with limited attention to how the expression of descriptions influences downstream performance.

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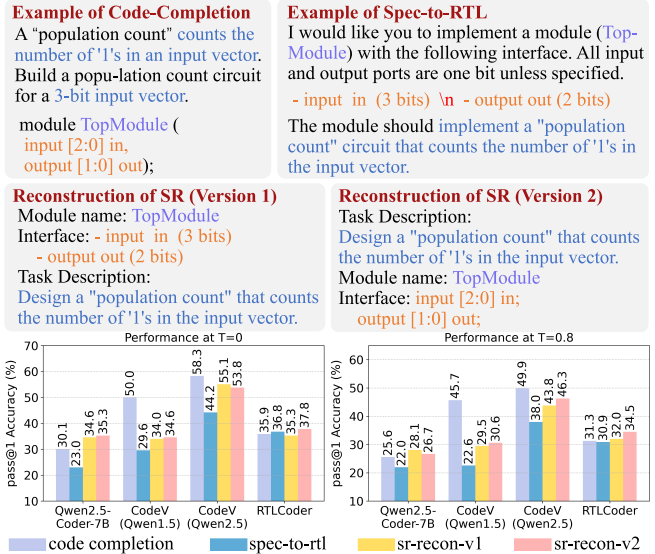


Figure 1: Descriptions of the Code-Completion (CC) and Spec-to-RTL (SR) tasks in the VerilogEval-v2 are equal in design intent but differ in structure. The top shows an example, and the bottom reports model performance. Results indicate that expression structure strongly affects performance: SR-Recon consistently outperforms SR, and CC benefits CodeVs under more constrained input formats.

In practice, free-form natural language descriptions of hardware design from users often suffer from ambiguity in intent, redundancy in expression, and irregularity in structure, particularly in critical modules involving sequential logic, finite state machines (FSMs), and complex control behaviors (Liu et al. 2025). Thus, crucial information is often scattered, underspecified, or only implicitly conveyed through the text, posing significant challenges for the model to organize and understand the necessary semantics. In contrast, Verilog is a formal specification language for modeling hardware circuits, characterized by strict structural constraints, strong semantic rigor, and high demands for domain expertise (Pei et al. 2024). Such gap reveals a fundamental challenge in Verilog code generation task: transforming from a highly expressive and inherently unstructured de-

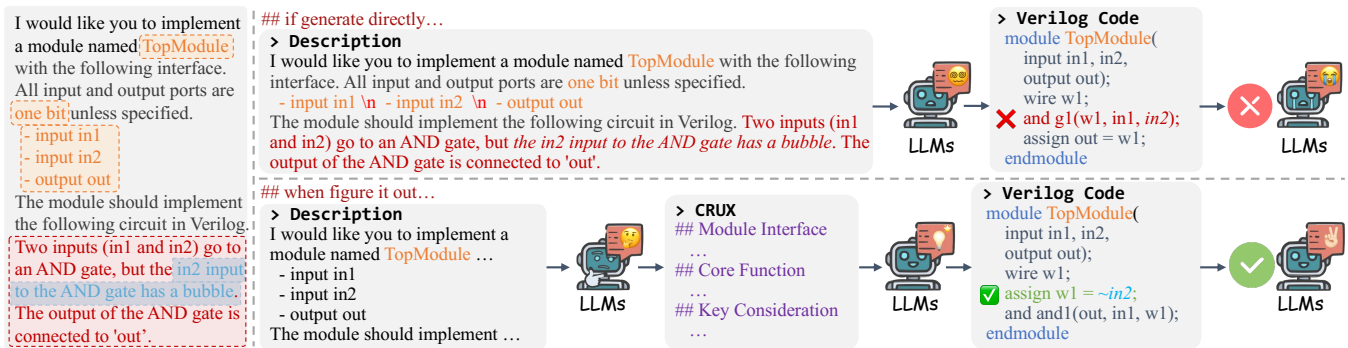


Figure 2: An example from the VerilogEval-v2 Spec-to-RTL benchmark illustrates that the original description underemphasizes critical design details, often leading LLMs to incorrect implementations. Although the model is capable of generating correct code, ambiguity in the input hinders accurate realization. In contrast, providing the model with CRUX enables more reliable alignment with the desired design intent, thereby leading to more precise implementations.

scription space into a structured code space governed by syntactic rigidity, modular hierarchy, and functional alignment. The high difficulty of this transformation poses significant obstacles to existing LLM-based approaches, often resulting in misaligned design intent, semantic drift, and distorted implementations in engineering.

Motivated by this gap, we investigate the effect of input formulation and find semantically structured and refined expressions leading to better generation performance. As illustrated in Figure 1, even when the descriptions of the two tasks contain the same underlying information, the model’s performance can vary substantially depending on how the information is expressed. Notably, when the original input of Spec-to-RTL (Pinckney et al. 2025) is restructured to expose its key components more explicitly and precisely, the models demonstrate significant improvements in generation accuracy, suggesting the importance of input clarity and organization in guiding LLMs toward robust code generation.

Based on the analysis above, we propose **C**ore **R**efined **U**nderstanding **e**Xpression (CRUX), which serves as a structured intermediate space that narrows the gap between free-form descriptions and formal Verilog implementations. The CRUX space captures the essential semantics of the user intent while structuring the descriptions for Verilog code generation, offering a stable and precise foundation for producing synthesizable and correct implementations. CRUX comprises three key components: *Module Interface*, *Core Functions*, and *Key Considerations*, each addressing a distinct aspect of Verilog generation. Specifically, (i) The *Module Interfaces* establish the structural foundation for interface-compliant Verilog modules by explicitly defining the input and output ports along with their signal properties. (ii) The *Core Functions* capture the essential circuit behaviour logic, clearly specifying functional goals and guiding the overall control and data flow. (iii) The *Key Considerations* highlight subtle but critical implementation details and constraints to ensure the generated code is both synthesizable and accurate. Building on these components, CRUX provides a coherent engineering context and functional blueprint for hardware design, enabling precise code generation with respect

to structural completeness, behavioral fidelity, and synthesis feasibility, as shown in Figure 2.

To fully leverage the guiding potential of CRUX, we develop a comprehensive framework composed of two stages: *Joint Expression Modeling* and *Dual-Space Optimization*, as shown in Figure 3. In the first stage, we construct the CRUX through a combination of LLM-based generation and category-specific strategies, over a diverse set of descriptions reflecting real-world human usage. We then perform supervised fine-tuning (SFT) using both CRUX and Verilog code as supervision signals, enabling the model to establish an initial mapping from natural language descriptions to structured CRUX expressions, as well as the corresponding code generation capabilities. In the second stage, we introduce CRUX-enhanced GRPO, an RL-based procedure that jointly optimizes two interconnected spaces: the CRUX space and the Verilog code space. By going beyond the limitations of static supervision, this dual-space optimization enables the model to adaptively converge toward high-quality solution regions aligned with target design intents.

Comprehensive experiments on multiple Verilog generation benchmarks demonstrate that our model QiMeng-CRUX, achieves state-of-the-art performance across both general-purpose and Verilog-specific models, especially under challenging and realistic design scenarios like Spec-to-RTL (from 49.3% to 64.7% with T=0, from 46.8% to 64.4% with T=0.8) and RTLLM-v2 (from 50.9% to 63.8%). In addition, the CRUX space proves to be a robust and semantically meaningful intermediate guidance that enhances performance even when used as a prompt for other code models without any further training. These findings highlight the potential of CRUX as a powerful and effective approach for supporting precise Verilog code generation. Code is available at <https://github.com/Taskii-Lei/QiMeng-CRUX-V>.

Related Work

LLM-based Verilog code generation has attracted growing attention as researchers explore automated hardware design. Beyond general-purpose methods, recent work adapts generation paradigms to Verilog’s unique characteristics, span-

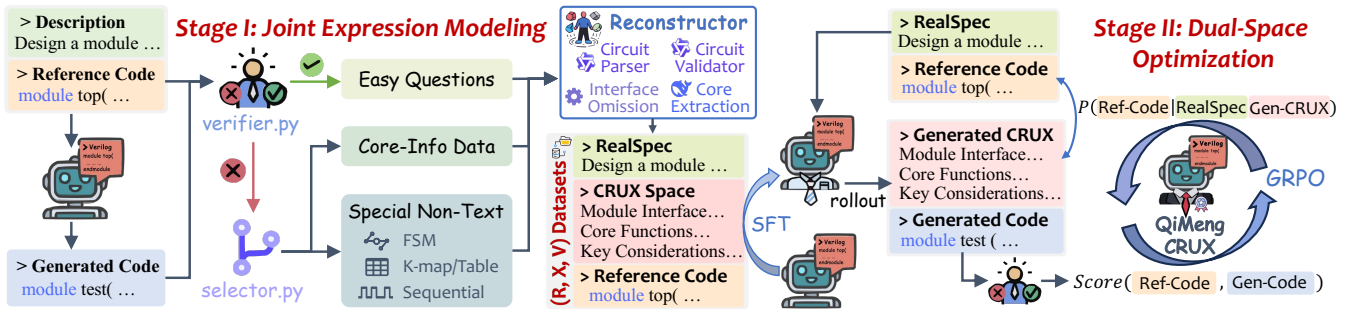


Figure 3: Overview of the two-stage training process. Stage I involves dataset categorization and reconstruction, which is used for supervised fine-tuning (SFT). Stage II applies CRUX-Enhanced GRPO for RL-based post-training.

ning directions such as dataset construction, framework design, feedback-driven optimization, and so on.

Dataset Construction and Enhancement High-quality datasets play a central role in Verilog code generation. Early work such as Dave (Pearce, Tan, and Karri 2020) fine-tuned GPT-2 to generate Verilog from natural language, marking one of the first attempts to align LLMs with hardware tasks. More recent studies mined public codebases and refined task descriptions (Liu et al. 2024b; Thakur et al. 2024; Zhao et al. 2025a). CraftRTL (Liu et al. 2025) further expanded data diversity by introducing non-text tasks like FSM. Other efforts including hdl2v (Hong et al. 2025) and MG-Verilog (Zhang et al. 2024), improved data quality through code translation and fine-grained annotation. These datasets collectively enhance both the scale and quality of Verilog training data.

Optimization via Feedback Given that Verilog code is ultimately executed and verified by downstream EDA tools, recent studies have explored two main strategies for incorporating feedback to improve generation quality. One line of work applies feedback at the inference stage, where either verification feedback (Wang et al. 2025a; Blocklove et al. 2025; Nakkab et al. 2024), or model feedback (Cui et al. 2024; Zhao et al. 2025b) is used to identify and revise incorrect outputs. The other line leverages RL-based post-training (Schulman et al. 2017; Bai et al. 2022; Shao et al. 2024; Yu et al. 2025) to optimize generation with reward functions (Le et al. 2022; Dou et al. 2024; Wang et al. 2024; Zhu et al. 2025), which may incorporate verification feedback, structural constraints, and design priors. This enables models to move beyond static supervision and align more closely with hardware-centric design objectives.

CoT Reasoning Motivated by the success of DeepSeek-R1 (Guo et al. 2025), which demonstrates the benefits of chain-of-thought (CoT) reasoning with RL, recent studies have tried to incorporate such diagram into Verilog code generation with verification feedback. Most CoT supervision is obtained through distillation from stronger models (Yubeaton et al. 2025; Qin et al. 2025; Zhu et al. 2025), while Wang et al. adopts optimization-based pipelines to construct thinking trajectories. While effective, CoT-based methods often require higher training costs and longer inference time compared to general models (Yang et al. 2025).

Methodology

Our goal is to generate structurally and functionally correct Verilog code from natural language descriptions by narrowing the gap between natural language descriptions and the Verilog code domain. To this end, we leverage CRUX as a domain-oriented intermediate space that explicitly captures core design intent and reformulates free-form descriptions into a domain-aligned structural form better supporting downstream code generation. We develop a two-stage training framework to support this process: *Joint Expression Modeling*, which jointly learns to generate both CRUX and Verilog from natural language descriptions, and *Dual-Space Optimization*, which further refines the CRUX and code quality through reinforcement learning in both spaces.

Joint Expression Modeling

To equip the model with the ability to construct CRUX and generate Verilog code, we begin with supervised fine-tuning (SFT). As existing datasets are largely synthetic and lack descriptive diversity, we augment the dataset of CodeV (Zhao et al. 2025a) by simulating real-world user phrasing via introducing variations, ambiguities, and structural incompleteness. Then we derive corresponding CRUX space to explicitly extract and organize the core design intent, resulting in a reconstructed dataset of triplets (R, X, V) , where R denotes the realistic task specifications (RealSpec), X is the CRUX, and V is the target Verilog code implementations. Finally, we perform SFT using both CRUX and Verilog code as learning targets. The model is trained to generate the CRUX first from the RealSpec, and then the Verilog code.

Corpus Categorization Given the diverse nature of Verilog tasks, we aim to identify which problems intrinsically require structural guidance beyond plain-text prompts. In particular, we are interested in a subset of circuit-specific tasks that cannot be adequately described or resolved through natural language alone, such as Karnaugh map interpretation, FSM modeling, or waveform analysis (Liu et al. 2025). To systematically explore this heterogeneity, we categorize the dataset into three types: *Easy Questions*, *Special Non-text* and *Normal Data*. We begin by prompting LLMs with task descriptions to generate corresponding Verilog code. Functional correctness is then automatically verified via testbenches comparing generated

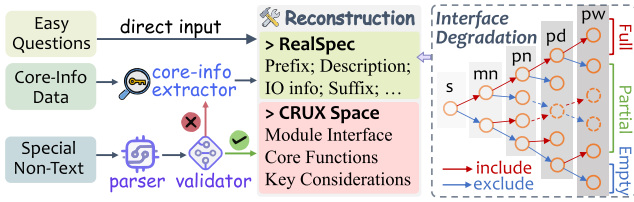


Figure 4: We apply different processing pipelines to the three categories. RealSpec uses prefix/suffix augmentation and interface degradation for variation, while CRUX is constructed mainly via LLMs. Abbreviations: s – start, mn – module name, pn – port name, pd – port direction, pw – port width.

outputs with references under identical inputs. Tasks passing verification are labeled Easy Questions. Among failures, those containing keywords such as “k-map”, “FSM”, or “sequential/waveform” are classified as Special Non-Text, with the rest assigned to Normal Data.

RealSpec Construction RealSpec is designed to simulate natural language descriptions that better reflect realistic distributions. While CodeV relies on synthetic prompts generated by ChatGPT, which inherently contain some noise, we introduce further variability to better match real-world conditions. Specifically, we parse each module’s header to extract detailed interface specifications (e.g., signal names, directions, and bit-widths), then selectively drop or retain parts of this information with a fixed probability, as shown in the right of Figure 4. The degraded interfaces are inserted into either the middle or the end of the original descriptions at a preset ratio. Particularly for Special Non-Text, we replace purely textual descriptions (as used in CodeV) with diagrams generated during the CRUX Deviation step, and only append the degraded interface at the end. Finally, we randomly add some prefixes and suffixes to ensure the fluency of the descriptions. Unlike CodeV’s fully specified prompts, RealSpec deliberately introduces interface degradation and controlled noise, pushing the model to infer missing components and thus improving robustness in realistic settings.

CRUX Derivation We define the CRUX space as comprising three components: *Module Interface*, *Core Functions*, and *Key Considerations*. The *Module Interface* comes from the reference code header, while the other two are derived differently depending on the corpus type, as illustrated in the left of Figure 4. (i) *Easy Questions*: The descriptions are considered sufficiently clear and complete, so we directly adopt them as *Core Functions*, leaving *Key Considerations* empty. (ii) *Normal Data*: As the primary source for constructing CRUX, these tasks are processed by prompting DeepSeek-R1 (Guo et al. 2025) with the descriptions and reference codes to extract and refine the *Core Functions* and *Key Considerations*. (iii) *Special Non-Text*: We use Qwen2.5-Coder-32B-Instruct (Hui et al. 2024) as a circuit parser to generate diagrams and concise analyses from both the description and code. This includes “State → Condition → Next State” for FSMs, logical expressions for K-maps or truth tables, and core behavior for sequential circuits. The

generated diagram and code are then validated by Qwen2.5-Coder-32B-Instruct. Only valid samples are retained to construct the RealSpec and CRUX, while parsing failures or incorrect cases are reclassified into *Normal Data* to process.

Ready and SFT After the steps above, we reconstruct the original dataset of CodeV (Zhao et al. 2025a) into (R, X, V) tuples and perform SFT to establish the LLM’s initial capacity for generating CRUX and correct Verilog code based on RealSpec.

Dual-Space Optimization

While SFT enables initial learning from static data, it often yields an under-refined CRUX space that lacks sufficient guidance for precise Verilog generation. So we introduce a Dual-Space Optimization framework that builds upon a CRUX-enhanced GRPO, where the model takes a RealSpec as input and rollouts both the CRUX and the corresponding Verilog implementation. Crucially, we design a composite reward that reflects two interconnected goals: (i) ensuring the generated code behaves correctly, and (ii) promoting CRUX space that better supports code generation.

The first goal is achieved by leveraging Code-Reward, which quantifies the functional correctness of the generated implementation. Specifically, we use the automated verifier to execute both the predicted and reference codes under identical input conditions and compute output matching scores. These scores reflect how well the generated code adheres to the intended behavior and serve as the basis for assigning reward signals during training.

For the second, rather than aligning the generated CRUX with a reference in a supervised manner, we use CRUX-Reward to measure how much it helps the model confidently arrive at a correct implementation. Intuitively, a well-formed CRUX should clearly identify the core design intent and filter out noise, thereby narrowing the gap with a more concentrated distribution centered on valid implementations.

In practice, we approximate this effect by computing the conditional sequence log-likelihood of the reference code given the RealSpec and the generated CRUX. To bound the reward within an interpretable range, we exponentiate the mean log-likelihood, yielding it as a direct measure of the model’s confidence: higher values indicate more concentrated distributions centered on valid implementations. Formally, given a training sample $(r, x, v_{ref}) \in (R, X, V)$, the model first rollouts the CRUX x' and then code c' conditioned on the RealSpec r . The CRUX-Reward is defined as:

$$\text{CRUX-Reward} = \exp \left(\frac{1}{L} \sum_{i=0}^{L-1} \log \pi_{\theta}(y_{i+1} \mid r, x', y_{0:i}) \right) \quad (1)$$

$$\text{where } y_i \in v_{ref}, \quad L = |v_{ref}|$$

This contrasts with conventional pipelines that optimize solely for final code correctness, often treating intermediate steps as auxiliary byproducts. Our formulation instead treats CRUX as one of the central modeling targets in the optimization loop, reinforcing its role as a structured intermediate space that bridges the intent and implementation.

Type	Model	VE-v1-Machine			VE-v1-Human			RTLLM-V1		
		p@1	p@5	p@10	p@1	p@5	p@10	p@1	p@5	p@10
Foundation General Models	GPT-4o	67.7	75.5	77.2	60.1	71.4	74.5	41.7	65.9	-
	Deepseek-V3-671B	77.6	86.2	87.4	70.7	77.4	78.8	60.9	74.2	-
Foundation Reasoning Models	Deepseek-R1-671B	81.0	87.4	89.5	81.5	87.6	88.5	64.8	82.9	-
	QWQ-32B	71.1	84.0	87.0	63.6	78.0	81.3	50.9	70.6	-
Verilog-Specific Reasoning Models	HaVen-7B	77.3	81.2	-	61.1	64.8	-	62.2	-	-
	CodeV-R1-Distill-7B	76.2	85.6	87.0	65.7	76.8	79.7	57.4	75.8	-
	CodeV-R1-7B	76.5	84.1	85.7	69.9	79.3	81.9	72.9	86.1	-
General Code Models	Qwen2.5-Coder-7B	50.1	66.5	70.9	22.9	36	39.5	32.2	48.2	56.0
	Qwen2.5-Coder-32B	66.6	76.6	79.7	47.6	58.1	61.8	47.9	67.7	-
	Deepseek-Coder-6.7B	52.2	55.4	56.8	30.2	33.9	34.9	30.2	44.0	52.5
Verilog-Specific General Models	RTLCoder-6.7B	61.2	76.5	81.8	41.6	50.1	53.4	35.8	40.3	43.1
	CodeV-Qwen1.5-7B	77.6	88.2	90.7	52.7	62.5	67.3	36.6	53.3	61.3
	CodeV-Qwen2.5-7B	77.3	87.9	90.1	57.9	66.7	69.7	39.3	63.5	74.2
	OriGen-7B	74.1	82.4	85.7	54.4	60.1	64.2	50.6	68.3	74.3
	VeriPrefer-7B	72.7	85.8	-	49.7	62.3	-	53.2	67.7	-
	QiMeng-CRUX-SFT-7B (Ours)	76.8	87.3	91.8	63.2	73.1	76.1	49.0	64.1	72.0
QiMeng-CRUX-Final-7B (Ours)	82.9	88.3	90.2	65.2	72.0	73.8	62.8	69.0	71.5	

Table 1: Main Results in VerilogEval-v1 and RTLLM-v1

Experiment

Experiment Settings

Datasets Our dataset is derived from the CodeV (Zhao et al. 2025a) corpus, which was constructed by hierarchically parsing Verilog code with GPT to obtain (Description, Verilog Code) pairs. They used the Rouge-L metric to measure the similarity between the dataset and the benchmark, and removed samples with Rouge-L > 0.5 to avoid data contamination. Following Corpus Categorization, we obtain about 40k Easy Questions, 18k Special Non-Text, and 107k Normal Data samples. During the Interface Degradation process, the complete interface is retained with a probability of 0.2, while all other variation elements are applied independently with a probability of 0.5. Only about 24k samples insert interface information in the middle of the description; the remaining samples include it only at the end.

Benchmarks To ensure a comprehensive evaluation, we adopt several representative and widely used Verilog generation benchmarks, including *VerilogEval-V1* (Liu et al. 2023), *VerilogEval-V2* (Pinckney et al. 2025), *RTLLM-V1* (Lu et al. 2024), and *RTLLM-V2* (Liu et al. 2024c). **VerilogEval-V1** consists of two sets of tasks: *Machine* (143 tasks automatically generated by GPT) and *Human* (156 hand-crafted tasks), both primarily aimed at evaluating code completion capabilities. Building upon this, **VerilogEval-V2** further enhances the quality and diversity by introducing two sub-tasks: *Code-Completion* that refined from V1-Human, and *Spec-to-RTL* which imposes additional requirements on the model’s ability to understand and generate core functional logic based on the specification. The **RTLLM** benchmark consists of four categories: *Arithmetic*, *Memory*, *Control*, and *Miscellaneous*, covering a wide range of challenges, including FSMs, combinational and sequential circuits, and long-text specifications. It poses a higher level of diffi-

culty compared to VerilogEval. RTLLM-V2 expands upon RTLLM-V1, increasing the total number of tasks from 29 to 50, with V1 forming a subset of V2. Since some prior works only report results on RTLLM-V1, we also include our performance on V1 for fair comparison.

Training Setup We adopt Qwen2.5-Coder-7B-Instruct (Hui et al. 2024) as the backbone model and follow the proposed two-stage framework, applying supervised fine-tuning (SFT) for 2 epochs with *LLaMaFactory* (Zheng et al. 2024) in Stage I, and CRUX-enhanced GRPO training for 1 epoch with *EasyRI* (Zheng et al. 2025) in Stage II.

Evaluation Setup Consistent with prior works, we adopt the *pass@k* metrics to assess generation performance, estimating the probability that at least one correct solution is obtained among *k* independent model outputs for each task, as defined in Equation 2. $n \geq k$ represents the number of independent solutions generated per task, and *c* corresponds to how many of these trials are functionally correct.

$$pass@k := \mathbb{E}_{\text{problems}} \left[1 - \frac{\binom{n-c}{k}}{\binom{n}{k}} \right]. \quad (2)$$

Notably, the original *VerilogEval-V2* paper requires reporting only *pass@1* under two settings to highlight practical LLM evaluation: a low-temperature setting (T=0.0, top_p=0.01, n=1) and a high-temperature setting (T=0.8, top_p=0.95, n=20) (Pinckney et al. 2025). However, many prior works still adopt a strategy of selecting the best performance among *Temperature = 0.2, 0.5, 0.8*. To enable fair comparison, we also include *pass@1* results under this strategy, denoted as *T-cross*. For the other benchmarks, we follow common practice and generate $n = 20$ independent solutions per task to compute *pass@1*, *pass@5*, and *pass@10*, reporting the best performance across T=0.2, 0.5, and 0.8.

Type	Model	VE-v2-CC (p@1)			VE-v2-SR (p@1)			RTLMLM-V2		
		T=0	T=0.8	T-cross	T=0	T=0.8	T-cross	p@1	p@5	p@10
Foundation General Models	GPT-4o	59.0	56.1	57.6	62.5	61.4	64.1	56.5	70.3	75.2
	Deepseek-V3-671B	68.0	66.1	68.7	68.8	66.9	62.4	59.1	71.5	73.3
Foundation Reasoning Models	Deepseek-R1-671B	82.7	81.0	79.1	83.3	79.8	77.5	64.7	75.8	79.7
Verilog-Specific Reasoning Models	HaVen-7B	-	-	-	-	-	54.6	-	-	-
	CodeV-R1-Distill-7B	-	-	65.6	-	-	65.2	57.2	71.9	77.1
	CodeV-R1-7B	-	-	69.9	-	-	68.8	68.0	78.2	81.7
General Code Models	Qwen2.5-Coder-7B	30.1	25.6	30.5	23.0	22.0	31.3	36.1	52.4	57.6
	Qwen2.5-Coder-32B	44.2	41.5	46.6	46.8	41.6	47.5	47.8	63.9	67.8
	Deepseek-Coder-6.7B	24.4	21.0	-	36.8	30.9	-	41.8	53.9	60.3
Verilog-Specific General Models	RTLCoder-6.7B	35.9	31.5	33.7	36.8	30.9	31.1	33.6	45.3	49.2
	CodeV-Qwen2.5-7B	58.3	49.9	60.4	44.8	37.4	42.2	41.0	60.1	68.1
	OriGen-7B	49.3	47.2	-	49.3	46.8	-	50.9	60.9	64.0
	QiMeng-CRUX-SFT-7B (Ours)	64.7	58.9	65.5	59.6	57.0	61.1	52.3	68.6	73.4
	QiMeng-CRUX-Final-7B (Ours)	68.0	66.7	67.6	64.7	64.4	64.2	63.8	70.6	73.9

Table 2: Main Results in VerilogEval-v2 and RTLMLM-v2

Main Results

Our main experimental results are presented in Table 1 and Table 2. We report the performance of Foundation Models (Liu et al. 2024a; Team 2025), General Code Models (Hui et al. 2024; Guo et al. 2024), and Verilog-Specific General Models (Liu et al. 2024b; Zhao et al. 2025a; Cui et al. 2024; Wang et al. 2025a). Given the remarkable performance of Reasoning Models in recent years, we separately group Deepseek-R1 (Guo et al. 2025) and Verilog-Specific Reasoning Models (Yang et al. 2025; Zhu et al. 2025).

It’s worth mentioning that our approach fundamentally differs from Reasoning-based methods. Chain-of-Thought (CoT) encourages iterative “generate-reflect-revise” cycles across multiple trajectories before reaching the final answer, whereas we explicitly outputs a structured expression of the core intent and implementation details, with only one-shot generation to the final code. This also affects token usage and computational cost: reasoning models typically require very long context windows of 16,384 tokens or more, while our model uses at most 4,096 tokens during both training and inference. Thus, our approach is categorized as a Verilog-Specific General Model for performance comparison. Moreover, although CodeV-R1 shares the *CodeV* name, it does not actually utilize the original CodeV dataset. Instead, it is built upon a newly constructed dataset from DeepSeek. Therefore, the improvements observed in CodeV-R1 and CRUX-V stem from different methods and data sources, and thus should not be directly compared.

For RTLMLM-v1 and v2, we evaluate the performance of RTLCoder, CodeV-Qwen1.5, and CodeV-Qwen2.5. And for VerilogEval-V2, we evaluate General Code and Verilog-Specified Models under the required settings 1) T=0.00, top_p=0.01, n=1 and 2) T=0.8, top_p=0.95, n=20 and report their *pass@1* results. The remaining results are derived from their own or prior works. Some entries in the table are left blank because the corresponding models are not open-

sourced, or they were not reported in their papers.

The main results demonstrate our QiMeng-CRUX model achieves the best *pass@1* performance across all benchmarks within both the General-Purpose Code Models and Verilog-Specific General Models, especially under challenging and realistic scenarios. It significantly outperforms GPT-4o on multiple tasks, most notably on RTLMLM-v2, where it achieves a *pass@1* of 63.8%, surpassing the previous SOTA by 12.9%, and outperforming Deepseek-V3, reaching performance comparable with Deepseek-R1. On VerilogEval-v2, QiMeng-CRUX brings substantial improvements over previous SOTA models across nearly all metrics, such as from 58.3% to 68.0% (+9.7%) in *pass@1* on the CC task, and from 49.3% to 64.7% (+15.4%) on the SR task. These results suggest that CRUX offers significant advantages in tackling complex code generation tasks and real-world design inputs.

Moreover, QiMeng-CRUX demonstrates robust performance across diverse task settings and specification styles. Originating from the CodeV Datasets, QiMeng-CRUX consistently performs better across tasks with diverse input forms and exhibits stronger robustness to specification variations than CodeV2.5. It achieves balanced performance across CC and SR (68.0% in CC and 64.7% in SR), avoiding the large gap observed in CodeV2.5 (58.3% in CC and 44.8% in SR). Furthermore, QiMeng-CRUX achieves substantial improvements across all metrics on the RTLMLM benchmark, highlighting the effectiveness and robustness of the CRUX methodology.

Ablation Study

In this section, we present a systematic ablation study of our CRUX framework within each of the two stages to assess the effectiveness of our methods. Plus, we investigate the transferability of the learned CRUX space to some general-purpose and verilog-specific code models to further evaluate its quality. The results are presented in Table 3 and Figure 5.

Stage	Model	VE-v1-Machine			VE-v1-Human			VE-v2-CC (p@1)		VE-v2-SR (p@1)		RTLLM-V2		
		p@1	p@5	p@10	p@1	p@5	p@10	T=0	T=0.8	T=0	T=0.8	p@1	p@5	p@10
Stage I	CodeV	77.3	87.9	90.1	57.9	67.6	69.7	58.3	49.9	44.8	37.4	41.0	60.1	68.1
	+ RealSpec	79.2	87.0	89.8	62.3	72.4	74.7	62.2	57.3	53.2	47.2	46.2	64.1	72.2
	+ CRUX	76.4	87.3	91.8	63.2	73.1	76.1	64.7	58.9	59.6	57.0	52.3	68.6	73.4
Stage II	w/o CRUX-Reward	80.6	87.2	91.4	61.7	69.3	73.1	61.5	59.5	62.8	58.3	59.5	73.0	74.8
	w CRUX-Reward	82.9	88.3	90.2	65.2	72.0	73.8	68.0	66.7	64.7	64.4	63.8	70.6	73.9

Table 3: Ablations of Both Stages

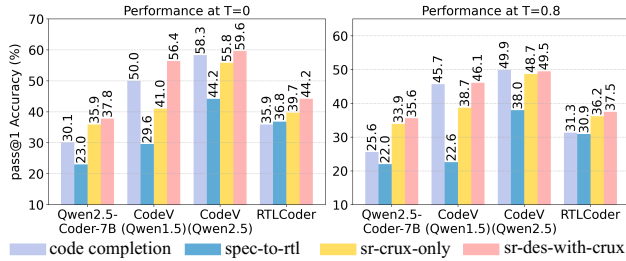


Figure 5: Using CRUX alone (crux_only) already leads to notable gains compared to using the original specification directly. Further combining CRUX with the original descriptions (des_with_crx) yields the best performance, even outperforming the Code-Completion task in most cases.

Ablation of RealSpec and CRUX in Stage I We focus on evaluating the impact of RealSpec and CRUX of Stage I. For clarity, we denote the original descriptions in CodeV as D , while R , X , and V follow the notation defined in *Joint Expression Modeling*. The groups are configured as: (i) CodeV: SFT on (D, V) ; (ii) CodeV + RealSpec: SFT on (R, V) ; (iii) CodeV + RealSpec + CRUX: SFT on (R, X, V) . In Table 3, results of Stage I demonstrate the benefits of RealSpec and CRUX. Compared to the baseline CodeV, incorporating RealSpec leads to consistent improvements across most benchmarks, especially on Spec-to-RTL, with $pass@1$ improving by 8.4% in T=0 and by 9.8% in T=0.8, indicating simulation of realistic input distributions enhances the model’s robustness and generalization to real-world usage patterns. Further introducing CRUX yields the best overall performance in Stage I, bringing at least a 5% improvement in $pass@1$ on both the SR and RTLLM-v2 benchmarks. Notably, RealSpec alone brings limited gains on the RTLLM, while CRUX continues to deliver clear improvements even under these more challenging settings, demonstrating its ability to capture core design intent and guide the model toward more precise Verilog generation. In summary, RealSpec improves robustness under natural prompt variation, and CRUX excels in tasks that require a deep understanding of core design intent and careful attention to implementation details.

Ablation of CRUX-Enhancement in Stage II We evaluate the impact of CRUX-Reward of Stage II by comparing models trained with and without it. As shown in Stage II of Table 3, introducing CRUX-Reward leads to a notable improvement in $pass@1$, while a slight drop in $pass@10$. A

similar trend can also be observed if compared with SFT models. This trade-off aligns with the general observation that RL-based methods typically improve generation precision at the cost of constrained solution diversity. Compared to GRPO without CRUX-Reward, incorporation of CRUX-Reward further steers the model towards more compact solution spaces that ensure both higher-quality CRUX and more precise Verilog code. These results highlight that CRUX functions not only as a structured expression but also as an inductive bias that shapes the model’s generation space toward more precise yet less diverse outputs.

Transferability of the Learned CRUX Space Beyond evaluating our model’s performance on Verilog benchmarks, we also investigate whether the learned CRUX space provides transferable benefits to general-purpose code models to assess its quality. Following the setup in Figure 1, we also conduct experiments on the Spec-to-RTL task to evaluate the guiding effect of CRUX as a prompt for general-purpose code models. Specifically, we test two settings: (i) using CRUX alone as the prompt, and (ii) appending CRUX as a bridge to the original descriptions. As shown in Figure 5, we observe consistent and sustained performance improvements under both settings, which reflect the quality of the learned CRUX space itself and further highlight its effectiveness in bridging natural language descriptions and precise code generation. These results confirm that the CRUX not only benefits our own model but also provides meaningful guidance to general-purpose or Verilog-specified code models, even without any additional training.

Conclusion

In this work, we present CRUX, a structured intermediate space designed to bridge the gap between free-form natural language descriptions and formal Verilog code. By explicitly modeling *Module Interfaces*, *Core Functions*, and *Key Considerations*, CRUX captures essential design intent and provides clear, targeted guidance for downstream code generation. Through a two-stage framework combining *Joint Expression Modeling* and *Dual-Space Optimization*, our method not only improves generation accuracy but also enhances the robustness and interpretability of large language models in hardware design tasks. Extensive evaluations show that QiMeng-CRUX achieves state-of-the-art performance across multiple Verilog benchmarks, demonstrating the effectiveness of semantically structured guidance in enabling precise and synthesizable HDL generation.

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